

Appl. No. 10/782,556  
Amdt. dated January 2, 2008  
Reply to Office action of October 1, 2007

### **REMARKS/ARGUMENTS**

Applicant would like to thank the Examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office Action, and the following remarks are presented for the Examiner's consideration.

Claims 1 and 6 were rejected under 35 U.S.C. 112, first paragraph as failing to comply with the written description requirement. The Office action later refers to claims 1 and 16. Since claims 1 and 16 are both independent claims, Applicant believes that the Examiner intended to reject claims 1 and 16, therefore, the rejection will be treated as such. Claim 16 has been cancelled. For the following reasons, the rejection is respectfully traversed as it applies to claim 1.

Regarding claim 1, each of the limitations is described in the specification. Specifically, the specification describes "A memory device" (see item 10 on page 6, line 26 to page 7, line 1) "comprising: a first tamper resistant memory" (see items 40 and 41 on page 7, lines 19-22) "which cannot be accessed directly by an electronic device" (see item 41 on page 8, lines 7-8). The specification also describes "a second non-tamper resistant memory" (see items 50 and 51 on page 9, lines 2-7) "which cannot be directly accessed by the electronic device" (see item 51 on page 8, lines 7-8). Further, the specification describes "wherein data stored in the first memory is saved to the second memory" (see page 15, lines 13-19). Therefore, since every limitation of claim 1 is sufficiently disclosed in the specification, Applicants respectfully request that the rejection be withdrawn as it applies to claim 1.

Claims 1-16 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,175,924 to Arnold. Claim 1 has been amended to better distinguish from the prior art. Claim 16 has been cancelled. For the following reasons, the rejection is rendered moot by the amendment.

Regarding amended claim 1, Arnold does not teach "a first tamper resistant memory which cannot be accessed directly by external electronic devices" and "a second non-tamper

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resistant memory which cannot be directly accessed by the external electronic devices,” as required. Arnold discloses a secure module (13) including a ROM (55), RAM (53), and a processor (51) (see Figure 1). There is no specific disclosure in the specification of Arnold as to whether the ROM (55) or the RAM (53) can be accessed directly by an external processor, such as the main microprocessor (15). However, Figure 1 depicts the main microprocessor (15), as well as other devices (21 and 25) being directly connected to the ROM (55) and the RAM (53) by a bus (17), which implies that direct access *is* available. Further, additional ROM (33) and RAM (31) are directly connected to the main microprocessor (15) by the bus 17. In any case, there is clearly no disclosure in Arnold of any memory that cannot be accessed directly by external electronic devices, as required by claim 1. Thus, claim 1 is not fully anticipated by Arnold. Further, since claims 2-15 depend from claim 1, they are not anticipated for the same reasons.

In consideration of the foregoing analysis, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any fees resulting from this communication, please charge same to our Deposit Account No. 16-0820, our Order No. NGB-36462.

Respectfully submitted,  
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January 2, 2008